AUTOMATIC SELECTION OF AN ON-CHIP ANCILLARY INTERNAL CLOCK GENERATOR UPON RESETTING A DIGITAL SYSTEM

Abstract of the Disclosure

A digital logic system includes a reset input for receiving a reset signal, and a clock input for receiving an externally generated main clock signal. An ancillary clock generator generates an ancillary clock signal. A clock selection multiplexer has a first input for receiving the externally generated main clock signal, a second input for receiving the internally generated ancillary clock signal, and an output for providing the externally generated main clock signal or the internally generated ancillary clock signal to a functional circuit. A resettable edge-triggered shift register has a first input for receiving the externally generated main clock signal, a second input for receiving the reset signal, and an output connected to the clock selection multiplexer for deselecting the internally generated ancillary clock signal and selecting the externally generated main clock signal after detecting a certain number of edges of the main clock signal following the reset signal.